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RAYTHEON COMPANY
C/O DALY, CROWLEY, MOFFORD & DURKEE, LLP
354A TURNPIKE STREET
SUITE 301A
CANTON, MA 02021

EXAMINER
NGUYEN, LEON VIET Q

ART UNIT	PAPER NUMBER
2635	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/04/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/511,862	WASHAKOWSKI ET AL.	
	Examiner	**Art Unit**	
	Leon-Viet Q. Nguyen	2635	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-23 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-14 and 16-23 is/are rejected.

7)☒ Claim(s) 15 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 15 October 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 12-23-04
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 12/23/2004 was filed after the mailing date of 12/23/2004. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Objections

2. Claims 3 and 12 objected to because of the following informalities:

Re claim 3, "corresponding to the the quadrature..." should read "corresponding to the quadrature..."

Re claim 12, "the sum and the difference" lack antecedent basis. For the purpose of this examination, the examiner will interpret the sum and the difference to be in reference to the sum and the difference of the first and second filter response values of claim 10.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claim 1-4, 7-8, 10-13, and 18-21 are rejected under 35 U.S.C. 102(b) as being anticipated over Young et al (US5570392). Furthermore, Young cross-references the details of RAM 322 and ROM 328 in US Pat. No. 5,440,506, which is hereby referred to as US5440506.

Re claim 1, Young discloses a method for shaping a baseband signal comprising:

providing a plurality of coefficient memories (322 and 328), each having a plurality of coefficients values representing filter response waveform values (col. 17 lines 29-34, col. 20 lines 28-30);

determining a coefficient memory address for each of the coefficient memories (col. 17 lines 29-34);

addressing each of the plurality of coefficient memories (it is inherent to assign a determined coefficient memory address to the coefficient memory);

retrieving an addressed coefficient value from each of the plurality of coefficient memories (col. 18 lines 51-53, it is inherent to retrieve a coefficient value from the memory to perform the incrementing and decrementing functions);

providing a negative value for each of the retrieved ones of the plurality of coefficient values (col. 19 lines 26-30);

selecting in response to the baseband signal, one of the retrieved coefficient value and the negative value (it is inherent that one of the coefficient values stored in memory be selected); and

summing the selected value from each coefficient memory (335) for providing a shaped signal (col. 3 line 65-col. 4 line 4).

Re claim 2, Young discloses a method of further comprising sharing the plurality of coefficient memories for shaping both an in-phase baseband signal and a quadrature baseband signal (col. 16 lines 12-29, the coefficient values stored in the ROM used in computation with the in-phase and quadrature branch of the signal).

Re claim 3, Young discloses a method wherein sharing the plurality of memories comprises:

retrieving one of the coefficient values corresponding to the in-phase baseband signal (col. 17 lines 45, c_0 is the coefficient value and $v_I(m)$ is the in-phase signal) on a first edge of a clock signal (col. 17 line 45, clock 0 is the first cycle/edge of the clock signal); and

retrieving one of the coefficient values corresponding to the the quadrature baseband signal (col. 17 lines 49-51, c_4 is the coefficient value and $v_Q(m+4)$ is the quadrature

signal) on a different second edge of the clock signal (col. 17 line 49, clock 1 is the second cycle/edge of the clock signal).

Re claim 4, Young discloses a method wherein the clock signal comprises a digital to analog converter clock signal (col. 1 lines 41-50, the signal is converted from analog to digital then reconstructed to an analog signal). Furthermore, it is inherent that a digital to analog converter have a clock signal to control the sampling rate.

Re claim 7, it is well known to one of ordinary skill in the art that 2's complement notation is one form of representing negative values.

Re claim 8, US5440506 discloses a method wherein providing a plurality of coefficient memories (202, col. 1 lines 35-36) comprises combining at least two filter coefficients for forming the plurality of coefficient values (fig. 3, it is inherent that 311 and 312 have some identifying address or coefficient. Furthermore it is inherent that coefficients input to differential amplifier 330 are combined and output some value) such that coefficient memory storage is minimized. Young discloses the use of ROM 328 to eliminate recoding hardware of multipliers connected to the ROM, interpreted as part of the memory storage.

Re claim 10, Young discloses a method wherein the plurality of coefficient memories further includes:

the sum of a first filter response value and a second filter response value (col. 16 lines 12-15, the data associated with a pair coefficient values of the is FIR filter, which is interpreted as the filter response value, is added together).

Re claim 11, Young discloses a method wherein the first filter response and the second filter response are symmetric (col. 16 lines 12-15).

Re claim 12, Young discloses a method wherein retrieving coefficient values comprises:

providing an address counter (326 and 330) having a plurality of logic outputs for addressing the coefficient memories (col. 18 lines 48-59, it is disclosed in fig. 2 of US5440506 is that the address generators coupled to RAM and ROM are the same); and

determining whether to retrieve one of the sum and the difference in response to selected ones of the logic outputs (col. 16 lines 12-16, selecting the sum and coefficient values addressed by the address generator to be multiplied together) .

Re claim 13, Young discloses a method further comprising:

providing a logic circuit (322) having an output, a first input coupled to a logic output of the address counter (the output of 326 to 322), a second input coupled to an in-phase data symbol bit (col. 19 lines 10-11) and a third input coupled to a quadrature data symbol bit (col. 19 line 12);

determining whether to select one of the retrieved value and the negative value in response to the output of the logic circuit (col. 19 lines 22-23, it is inherent that one of the coefficient values corresponding to the inputs is selected for reading and writing).

Re claim 18, Young discloses a method for shaping a baseband signal comprising:

providing a plurality of digital words (col. 16 lines 31-32), each digital word indicating a coefficient value at an instant of time (col. 16 lines 3-8, the words are stored in RAM 322, it is inherent that the words stored in 322 are assigned some coefficient value);

selecting responsive to the baseband signal, one of the digital words and a corresponding negative value of the digital word (col. 16 lines 24-25, col. 19 lines 26-30, the coefficients which are less than ¼ are multiplied by the words yielding a positive a negative word and it would be inherent to select those words for summing); and

summing the selected digital word (col. 16 lines 18-25) for providing a baseband shaped signal (col. 3 lines 65-67, col. 16 line 38).

Re claim 19, the claim limitations as recited have been analyzed and addressed in the above rejections with respect to claim 8. It is inherent to store the digital words in the same coefficient memory.

Re claim 20, Young discloses a device comprising:

a plurality of coefficient memories (322 and 328), each memory having an input address bus (it is inherent that a memory device have an address bus to determine the locations of the addresses from the address generator), a multiplexor input (fig. 3b from US5440506) and a coefficient value output (it is inherent that a memory device output values stored in memory which correspond to coefficients);

a plurality of first registers (fig. 16, the 3 byte shift registers), each having an input coupled to a respective one of the coefficient value outputs (fig. 16, the output from the dual port RAM), a digital to analog (D/A) clock input (106, 108, and 110, it is inherent that a digital down converter have a digital to analog converter and a digital to analog converter clock) and an output (fig. 16, the output of the register) ;

a plurality of negative value circuits (fig. 16, the byte subtracter), each circuit having an input coupled to a respective one of the first register outputs (fig. 16, the output of the 3 byte shift register to the byte subtracter), and an output (fig. 16, the out output of the byte subtracter);

a plurality of 2:1 multiplexors (fig. 16), each having a first input coupled to a respective one of the first register outputs (fig. 16, the output of the 3 byte shift register to the 2:1 multiplexors) and having a second input coupled to a respective one of the output of the plurality of negative value circuits (fig. 16, the output of the byte subtracter to the 2:1 multiplexor);

a plurality of second registers (fig. 17, 1724 and 1907), each having an input coupled to a respective one of the outputs of the plurality of 2:1 multiplexors (fig. 17, the output of 1708), a digital to analog (D/A) clock input (106, 108, and 110, it is inherent that a digital

down converter have a digital to analog converter and a digital to analog converter clock) and an output (fig. 17, the outputs of 1724 and 1907); and

an adder (fig. 17, the byte adder) having a plurality of inputs coupled to respective ones of the plurality of second registers (fig. 17, the outputs of 1724 and 1907).

Re claim 21, Young discloses loading control words that are in two's complement and signed magnitude format (fig. 24) into a decoder (col. 3 lines 46-49) which is coupled to the byte subtracter of fig. 16. It is inherent that the byte subtracter have a two's complement and signed magnitude logic element to perform an operation on the control word.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Young et al (US5570392) as applied to claim 1 above, and further in view of Vinekar (US6031431).

Re claim 5, Young fails to teach the coefficient memory address as claimed.

However Vinekar teaches the method wherein determining a coefficient memory address comprises:

determining an increment for providing a predetermined number of samples for each of a plurality of symbols comprising the baseband signal (col. 5 lines 51-55, col. 5 line 65-col. 6 line 3, the step size control circuit used for incrementing the address counter); and incrementing an address counter in response to the predetermined number of samples for each symbol and a predetermined coefficient memory size (col. 6 lines 20-27).

Therefore taking the combined teachings of Young and Vinekar as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the step size control circuit and address counter of Vinekar into the phase generator of Young to support multiple interpolation rates with the values stored in memory (col. 6 lines 28-33) and perform pulse shaping operations on in-phase and quadrature signals (col. 3 lines 17-21).

7. Claim 6 rejected under 35 U.S.C. 103(a) as being unpatentable over Young et al (US5570392) as applied to claim 1 above, and further in view of Glas et al (US6560296B1).

Re claim 6, Young fails to teach the method as claimed. However Glas teaches a method wherein the baseband signal comprises an in-phase signal and a quadrature signal (fig. 6, it is inherent that a baseband signal comprise of I and Q signals); wherein selecting the coefficient value comprises selecting an in-phase value in response to the in-phase signal (col. 4 lines 23-26, a response from the in-phase digital

data signal combined with the oscillator is expected) and selecting a quadrature value in response to the quadrature signal (col. 4 lines 23-26, a response from the quadrature-phase digital data signal combined with the oscillator is expected); and

wherein summing the selected value comprises summing the selected in phase value from each coefficient memory (fig. 6, CEI1 and CEI2 summed together in 20) for providing a shaped in phase signal (I-RF OUT), and summing the selected quadrature value from each coefficient memory (fig. 6, CEQ1 and CEQ2 summed together in 20) for providing a shaped quadrature signal (Q-RF OUT).

Therefore taking the combined teachings of Young and Glas as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the method of combining I and Q signals of Glas into the phase generator of Young to perform QPSK modulation (col. 2 lines 46-47) which requires half the bandwith of BPSK modulation (col. 1 lines 46-47) and therefore increasing efficiency.

8. Claim 9 rejected under 35 U.S.C. 103(a) as being unpatentable over Young et al (US5570392) as applied to claim 1 above, and further in view of Iwamatsu et al (US5648988).

Re claim 9, Young fails to teach a method wherein providing a plurality of coefficient memories further comprises providing coefficient memories corresponding to a plurality of roll-off factors. However Iwamatsu teaches first and second memory devices (col. 2 lines 63-67) that comprise of tap rating ratios output to roll-off filters (col. 2 line 62-col. 3 line 6).

Therefore taking the combined teachings of Young and Iwamatsu as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the memory devices of Iwamatsu into the phase generator of Young to detect a location of a cause of deterioration of pulse forms (col. 3 lines 11-12) and provide for pulse shaping.

9. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Young et al (US5570392).

Re claim 14, Young discloses a method wherein summing the selected value comprises:
providing a plurality of adder stages (808, fig. 9, col. 8 lines 15-17), each adder coupled to a pipeline register (fig. 8); clocking the pipeline register at a digital to analog converter (D/A) rate (Young does not explicitly state using the D/A rate. However it would have been obvious to one of ordinary skill in the art to use the rate of the D/A converter in lines 41-50, which decreases the sampling rate without loss of information, to clock the registers); and scaling and formatting the summed values (341) after a final adder stage (810). It is noted that Young discloses a standard multiplier design in fig. 8, which is taken to be the equivalent of the multipliers 332 and 333.

10. Claims 16-17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Young et al (US5570392) as applied to claim 1 above, and further in view of Stanley et al (US20020141440).

Re claim 16, Young fails to teach a method wherein the filter waveform comprises a raised cosine. However Stanley teaches a low-pass finite impulse response filter with a square-root raised cosine response (¶0103). It would have been obvious and necessitated to use a raised cosine filter.

Therefore taking the combined teachings of Young and Stanley as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the filter of Stanley into the phase generator of Young to reduce inter-symbol interference (¶0103).

Re claim 17, the claim limitations as recited have been analyzed and addressed in the above rejections with respect to claim 16.

11. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Young et al (US5570392) as applied to claim 20 above, and further in view of Rhines et al (US5392299).

Re claim, Young teaches a device further comprising a coefficient address generator (326 and 330) having an output coupled to a coefficient memory input address bus (the output from the address generator be coupled to the address bus of the memory device to assign addresses to memory locations is expected). However, Young fails to teach the input address having a plurality of address lines. Rhines teaches an address bus comprised of a column address line and a row address line (col. 13 lines 50-56).

Therefore taking the combined teachings of Young and Rhines as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the method of having a plurality of address lines into the phase generator of Young so that an address counter can access every location in a data plane and retrieve any individual symbol in a codeword (col. 16 lines 62-65).

12. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Young et al (US5570392) as applied to claim 22 above in view of Rhines et al (US5392299) and further in view of Keevil et al (US20030142764A1).

Re claim 23, Young and Rhines fail to teach the limitations as claims. However Keevil teaches a device wherein the coefficient address generator further comprises:
an adder having a plurality of address output lines (¶0031, an adder for adding the incrementation value to the previous address);
an address register coupled to the plurality of address output lines (¶0031, an accumulator for storing previously generated addresses) and having clocked address line outputs (fig. 35, it would have obvious and necessitated that the output address be clocked by CLK) and an address counter most significant bit output (352, ¶0230, the multiplexor 352 selects the two most significant bits and outputs them);
an exclusive or logic gate array (fig. 35, it would have been obvious to one of ordinary skill in the art to use XOR gates instead of OR gates to implement binary addition) having address inputs coupled to the clocked address lines outputs (fig. 35, the inputs of the OR gates coupled to OUT_ADDRESS 398 which is clocked by CLK) and an

address counter most significant bit input coupled to the address counter most significant bit output (¶0230, multiplexor 352 selects the two most significant bits and has outputs relating to the input state. One of ordinary skill in the art would realize that the input and output are coupled in the multiplexor), and outputs coupled to a corresponding plurality of the plurality of address lines of the coefficient memory address bus (fig. 35, 398, it would have been obvious and necessitated to have the output of the address generator coupled to the coefficient memory previously rejected in claim 22); and

an XOR multiplexor (366, it would have been obvious to one of ordinary skill in the art to use XOR instead of OR to implement binary addition) having inputs coupled a pair of baseband bit signals (fig. 34, the inputs 1 and 2 to 366) and an output coupled to one of the plurality of address lines of the coefficient memory address bus (fig. 34, the output of 366 to ROM 310 of fig. 29B).

Therefore taking the combined teachings of Young, Rhines, and Keevil as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the address generator of Keevil into the phase generator of Young and Rhines to reduce the size of the RAM needed by 50% (¶0234) and thereby decrease the overall hardware size.

Allowable Subject Matter

13. Claim 15 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The allowable subject matter pertains to using the D/A rate divided by the symbol rate to attain the number of retrievals per coefficient.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leon-Viet Q. Nguyen whose telephone number is 571-270-1185. The examiner can normally be reached on monday-friday, alternate friday off, 7:30AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vu Le can be reached on 571-272-7332. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Leon-Viet Nguyen/

VU LE
SUPERVISORY PATENT EXAMINER